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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/895,306	AU ET AL.	
	Examiner	Art Unit	
	Eric Chang	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/09/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12/7/01* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-31 are pending.

Specification

2. The disclosure is objected to because of the following informalities: several minor typographic errors in specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14, 17-19, 22-26 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,994,920 to Narayana et al. (hereafter referred to as Narayana '920) in view of U.S. Patent 5,955,897 to Narayana et al. (hereafter referred to as Narayana '897).

5. As to claim 1, Narayana '920 discloses an apparatus receiving a first read clock (26), a first write clock (22), a first look-ahead signal (20), a second read clock (40), a second write

clock (36), a second look-ahead signal (34) [col. 8, lines 20-30] to produce an output signal (HF) indicating if a FIFO is half-full or not half-full [col. 8, lines 32-33].

Narayana '920 also discloses a state machine (11) that is configured to receive a number of inputs including a look-ahead signal, a first and second read and write clock to produce an output signal indicating if a FIFO is half-full or not half-full [col. 6, lines 45-55]. Narayana '920 further discloses an apparatus that uses two state machines (12 &14), and a latch (16) to generate a FIFO half-full signal based on the input of a programmable look-ahead signal, and a first and second read and write clocks [col. 6, lines 58-67, and col. 7, lines 1-2].

Narayana '920 teaches all of the limitations, including a state machine that indicates when a FIFO is half-full and when said FIFO is not half-full, but does not teach that state machine indicates when a FIFO is almost full and when said FIFO is not almost full.

Narayana '897 teaches a state machine indicating a fullness of a FIFO similar to that of Narayana '920. In addition, Narayana '897 teaches that a state machine indicates when a FIFO is almost full and when said FIFO is not almost full [FIG. 3, and col. 3, lines 5-11].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the almost-full state machine as taught by Narayana '920. One of ordinary skill in the art would have been motivated to do so that the almost-fullness of the FIFO could be determined.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of using a state machine to determine a level within a FIFO. Moreover, the almost-full state machine means taught by Narayana '897 would improve the flexibility of Narayana '920 because it allowed for different

levels within the FIFO to be determined in addition to the half-empty status, depending on the type of state machine used.

6. As to claim 2, Narayana '920 discloses an apparatus comprising:

[a] a first set state machine (12) receiving a first read clock (26), a first write clock (22), a first look-ahead signal (20) [col. 8, lines 20-24], and a first control signal (28) [col. 2, lines 50-52] to produce a first set_output signal (30) [col. 8, lines 20-24];

[b] a second set state machine (14) receiving a second read clock (40), a second write clock (36), a second look-ahead signal (34) [col. 8, lines 25-30], and a second control signal (42) [col. 3, line 19] to produce a second set_output signal (32) [col. 8, lines 25-30];

[c] a synchronizer (19) coupled to said second set state machine, receiving said first read control signal and a reset signal to produce a synchronized output signal [FIG. 1 element 19, and col. 4, lines 1-5];

[d] a latch (16) receiving the first set_output signal and the synchronized output signal to produce a first latch_output signal indicating the FIFO half-full and a second latch_output signal indicating the FIFO is not half-full [col. 8, lines 32-33];

[e] a first logic block (15) receiving the second latch_output signal to produce the first control signal [col. 2, lines 53-55]; and

[e] a second logic block (18) receiving the first latch_output signal to produce the second control signal and the reset signal to the synchronizer.

Narayana '920 teaches an apparatus that uses two state machines, a synchronizer, a latch, and two logic blocks as claimed to generate a FIFO half-full signal based on the input of a first

and second read clocks, write clocks, and programmable look-ahead signals. Narayana '897 teaches that state machines indicating when a FIFO is almost full and when said FIFO is not almost full may likewise be used [col. 3, lines 5-11], substantially as claimed.

7. As to claim 3, Narayana '920 discloses a synchronizer apparatus further including an SR latch (19) receiving said second set_output signal from the second set state machine configured to receive a reset signal from the second logic block [col. 2, lines 53-55]. Narayana '920 teaches that the synchronization method further receives an external timing signal that controls the presentation of the second set_output signal from the SR latch [FIG. 1 element 22, col. 2, lines 45-47]. However, Narayana '920 teaches that the presentation is handled internally by the first state machine instead of using a flip-flop external to said state machine [col. 3, lines 37-39]. It would be obvious to one of ordinary skill in the art to use a read enabled clock within the state machine instead of an external flip-flop to control the presentation of the synchronization signal because it results in the same presentation of the signal to the workings of the state machine.

8. As to claim 4, Narayana '920 discloses the external timing signal for the synchronizer comprises a free running write clock signal [col. 2, lines 45-47].

9. As to claim 5, Narayana '920 discloses that the FIFO comprises a synchronous FIFO [col. 8, lines 38-39].

10. As to claim 6, Narayana '920 discloses the first write clock comprises a first write-enabled clock [col. 7, lines 25-26].

11. As to claim 7, Narayana '920 discloses the first read clock comprises a first read enabled clock [col. 7, lines 23-24].

12. As to claim 8, Narayana '920 discloses the second write clock comprises a second write-enabled clock [col. 7, lines 25-26]. Narayana '920 teaches that the second read and write clocks may be the same or different from the first read and write clocks, so the second write clock may also be a write enabled clock [col. 8, lines 29-31].

13. As to claim 9, Narayana '920 discloses the second read clock comprises a second read enabled clock [col. 7, lines 23-24]. Narayana '920 teaches that the second read and write clocks may be the same or different from the first read and write clocks, so the second write clock may also be a write enabled clock [col. 8, lines 29-31].

14. As to claim 10, Narayana '920 discloses a first delay block configured to provide a first predetermined delay to said first set_output signal [FIG. 1 element 18, and col. 2, lines 42-43].

15. As to claim 11, Narayana '920 discloses a second delay block configured to provide a second predetermined delay to said second set_output signal [FIG. 1 element 15, and col. 2, lines 54-55].

16. As to claim 12, Narayana '920 discloses a delay block including a predetermined delay configured during fabrication [col. 7, lines 27-33].

17. As to claim 13, Narayana '920 discloses a delay block wherein the predetermined delay is programmable [col. 7, lines 27-35].

18. As to claim 14, Narayana '920 discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58].

19. As to claim 17, Narayana '920 discloses a delay block including a predetermined delay configured during fabrication [col. 7, lines 27-33].

20. As to claim 18, Narayana '920 discloses a delay block wherein the predetermined delay is programmable [col. 7, lines 27-35].

21. As to claim 19, Narayana '920 discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58].

22. As to claim 22, Narayana '920 discloses a method for determining the emptiness of a memory buffer comprising: generating a half-full flag in response to a plurality of signals comprising a first and second read, write, and look-ahead signals [col. 8, lines 20-31]; generating a not half-full flag in response to same [col. 3, lines 4-6]; and presenting said signals to a state machine that generates an half-full flag [col. 8, lines 20-31]. Narayana '897 teaches that state machines indicating when a FIFO is almost full and when said FIFO is not almost full may likewise be used [col. 3, lines 5-11].

23. As to claim 23, Narayana '920 discloses that the generation of the fullness output flag is delayed by a time delay [col. 3, lines 51-54].

24. As to claim 24, Narayana '920 discloses that the generation of the not fullness output flag is delayed by a time delay [col. 3, lines 51-54]. Because Narayana '920 teaches that the not fullness output flag is generated at the same time as the fullness flag, a delay in the generation of the fullness flag also delays the not fullness flag.

25. As to claim 25 and 26, Narayana '920 discloses a programmable time delay in the generation of the fullness output flag and the not fullness output flag [col. 3, lines 51-54].

26. As to claim 29, Narayana '920 discloses an apparatus comprising: the first manipulating means [FIG. 1 element 12, col. 2, lines 50-52, and col. 8, lines 20-24]; the second manipulating means [FIG. 1 element 14, col. 3, line 19, and col. 8, lines 25-30]; the synchronizer [FIG. 1

element 19, and col. 4, lines 1-5]; the latch [col. 8, lines 32-33]; the first logic [FIG. 1 element 15, and col. 2, lines 54-55]; and the second logic [FIG. 1 element 18, and col. 2, lines 42-43].

27. As to claim 30, Narayana '920 discloses a first delay means to increase the pulse width of the first output signal [FIG. 1 element 18, and col. 2, lines 42-43].

28. As to claim 31, Narayana '920 discloses second delay means to increase the pulse width of the second output signal [FIG. 1 element 15, and col. 2, lines 54-55].

29. Claims 15-16 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,994,920 to Narayana et al. (hereafter referred to as Narayana '920) in view of U.S. Patent 5,955,897 to Narayana et al. (hereafter referred to as Narayana '897), and in further view of U.S. Patent 5,231,314 to Andrews.

30. As to claims 15-16, 20-21 and 27-28, Narayana '920 discloses that the delay block may be implemented either electronically or through discrete digital components without departing from the scope of the reference [col. 3, lines 54-58]. Thus Narayana '920 and Narayana '897 teach all of the limitations of the claim, but do not teach that the delay block may comprise a JTAG programmable delay block and other JTAG circuitry and instructions.

Andrews teaches that a JTAG programmable delay block may be used as a delay block in circuitry [col. 1, lines 41-53]. Thus, Andrews teaches a delay block similar to that of Narayana

'920 and Narayana '897. Andrews further teaches that the delay block may be implemented as a JTAG programmable delay block, substantially as claimed.

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the JTAG programmable delay block as taught by Andrews. One of ordinary skill in the art would have been motivated to do so to ensure reliable timing adjustment to compensate for clock skew [col. 1, lines 25-40].

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of implementing a timing delay block. Moreover, the JTAG programmable delay block means taught by Andrews would reduce the circuit complexity of Narayana '920 and Narayana '897 because it allowed for reliable timing without the need of separate set of test instrumentation [col. 1, lines 54-67].

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

ec
August 12, 2004

A. ELAMIN
PRIMARY EXAMINER